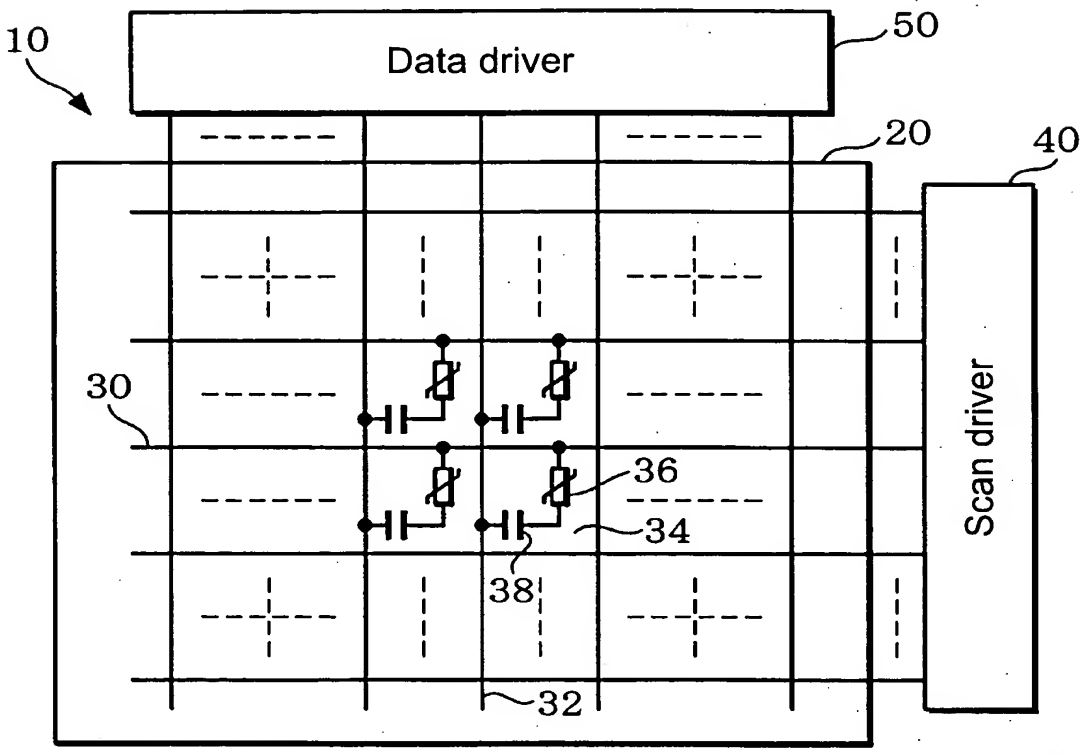
10
Data driver
50
20
40
30
36
34
38
32
Scan driver

FIG.1A

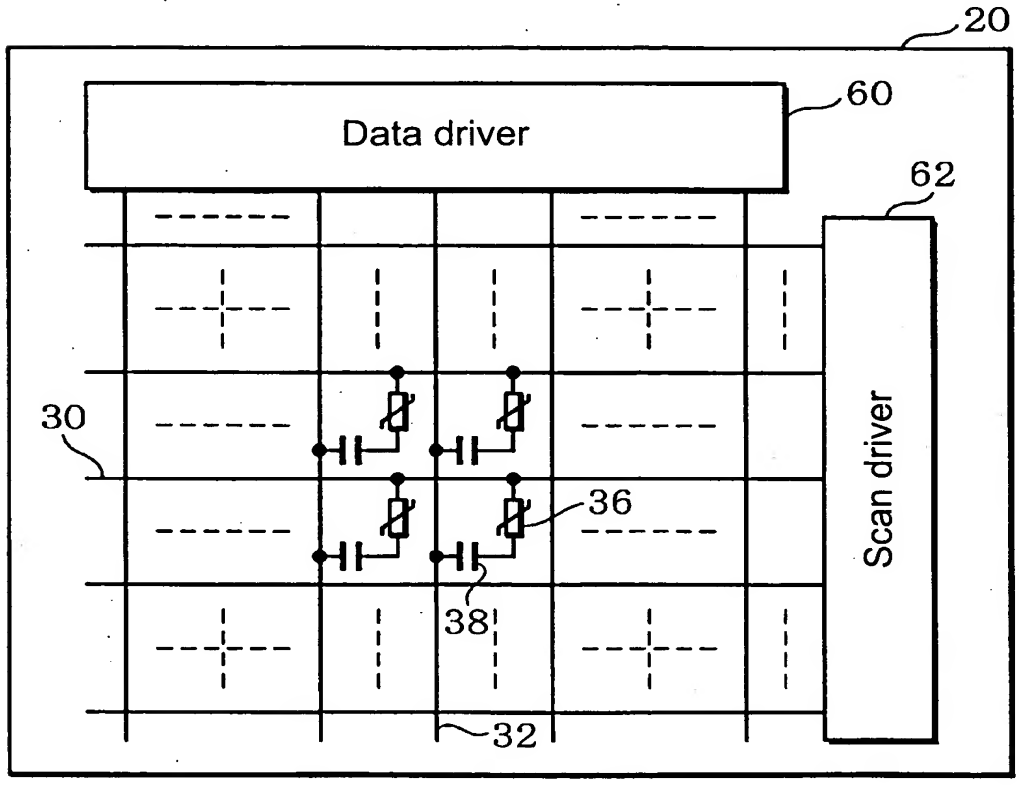
20
60
Data driver
62
30
36
38
32
Scan driver

FIG.1B

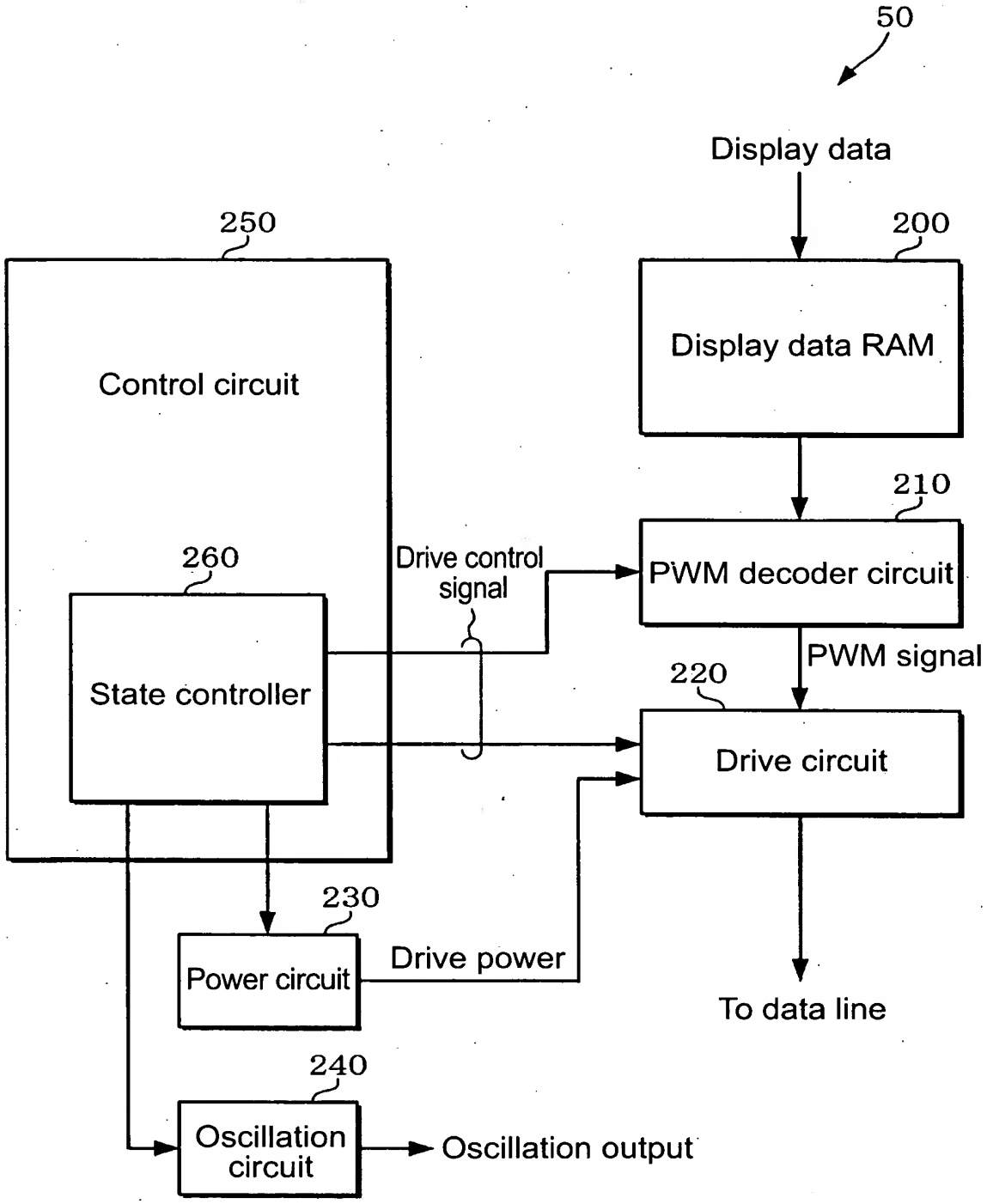
50
Display data
250
200
Control circuit
Display data RAM
210
260
Drive control signal
PWM decoder circuit
PWM signal
220
State controller
Drive circuit
230
Power circuit
Drive power
To data line
240
Oscillation circuit
Oscillation output

FIG. 2

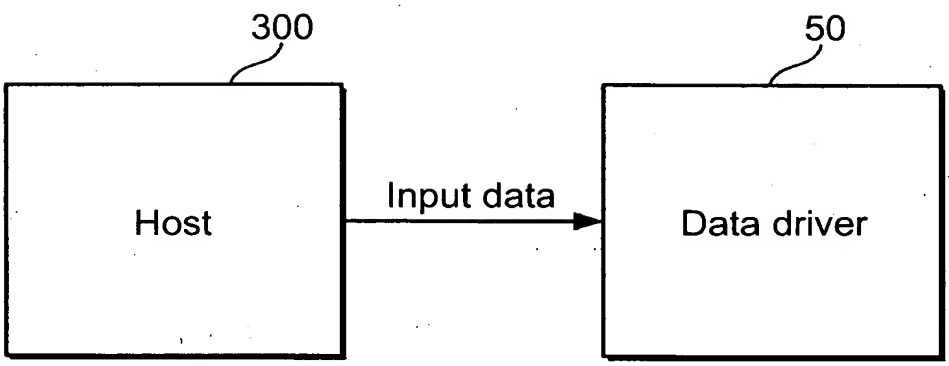

FIG. 3

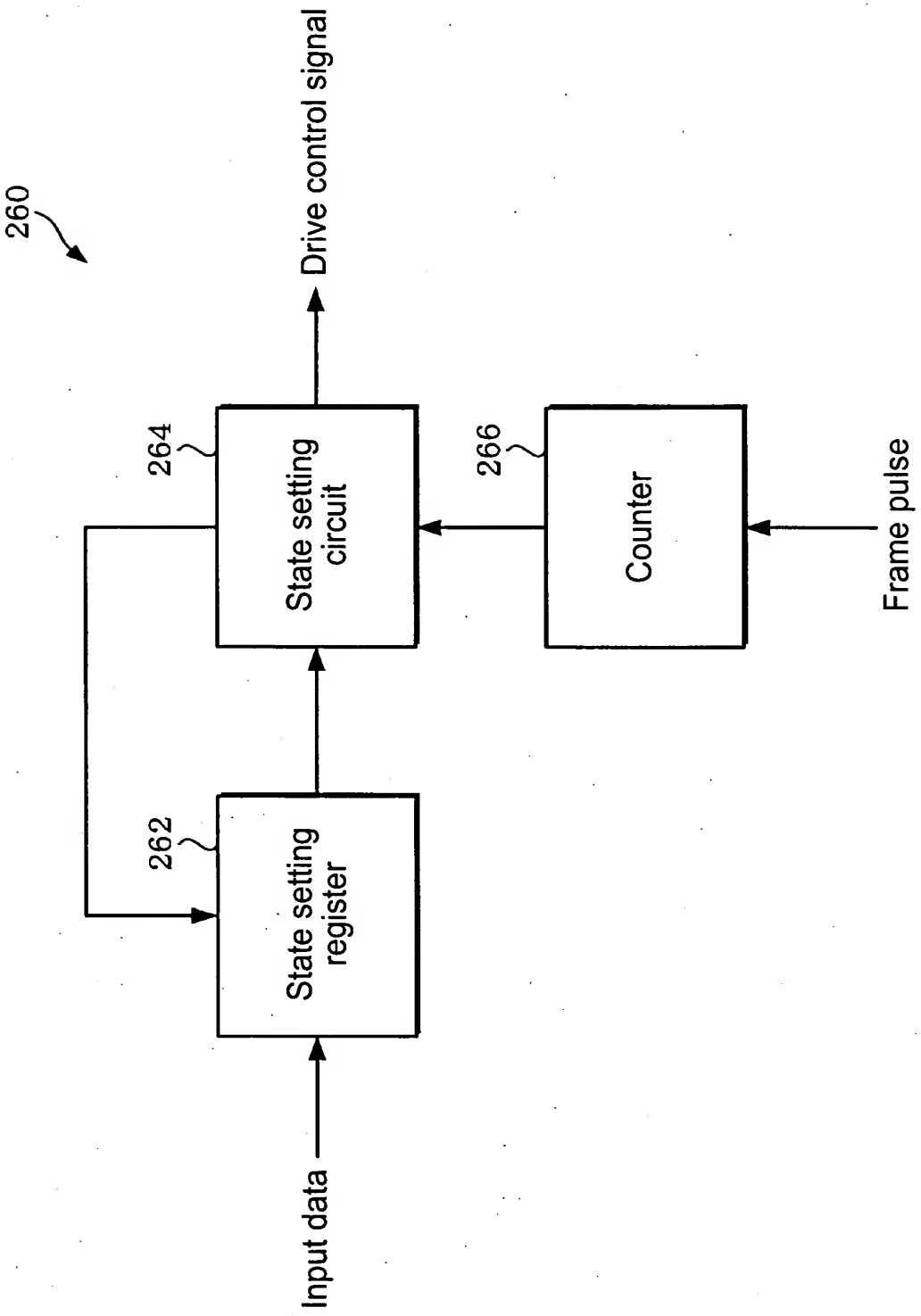
260
Drive control signal
264
State setting circuit
266
Counter
Frame pulse
262
State setting register
Input data

FIG. 4

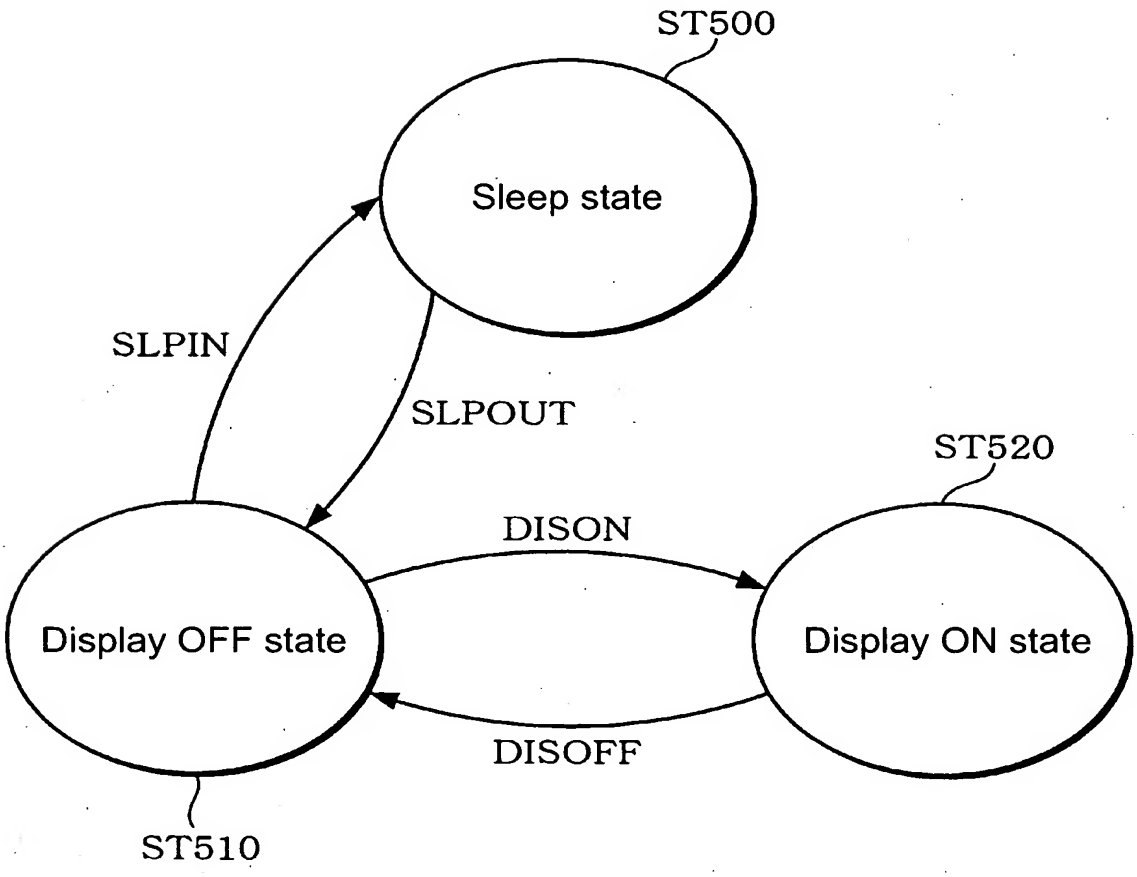
ST500
Sleep state
SLPIN
SLPOUT
ST520
DISON
Display OFF state
Display ON state
DISOFF
ST510

FIG. 5

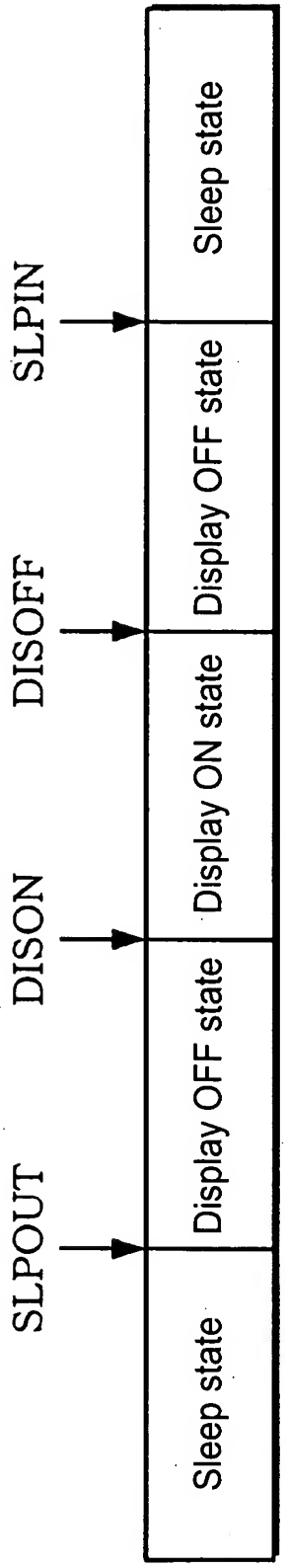
SLPIN
DISOFF
DISON
SLPOUT
Sleep state
Display OFF state
Display ON state
Display OFF state
Sleep state

FIG. 6A

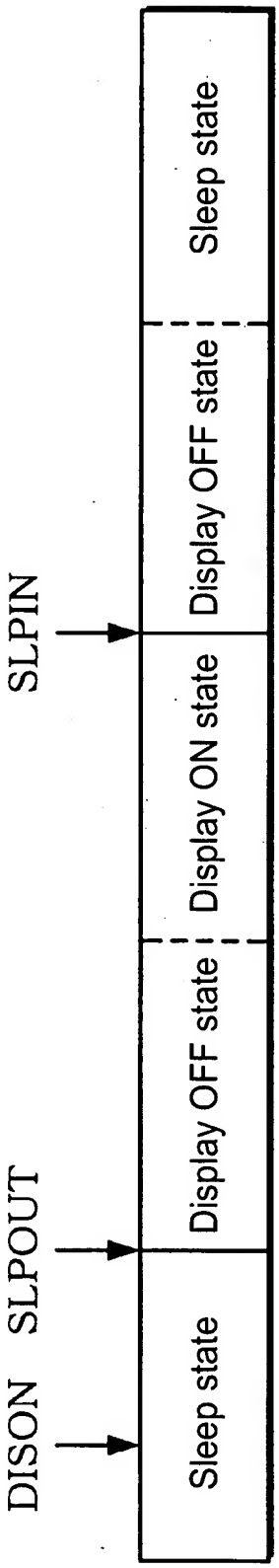
SLPIN
DISON
SLPOUT
Sleep state
Display OFF state
Display ON state
Display OFF state
Sleep state

FIG. 6B

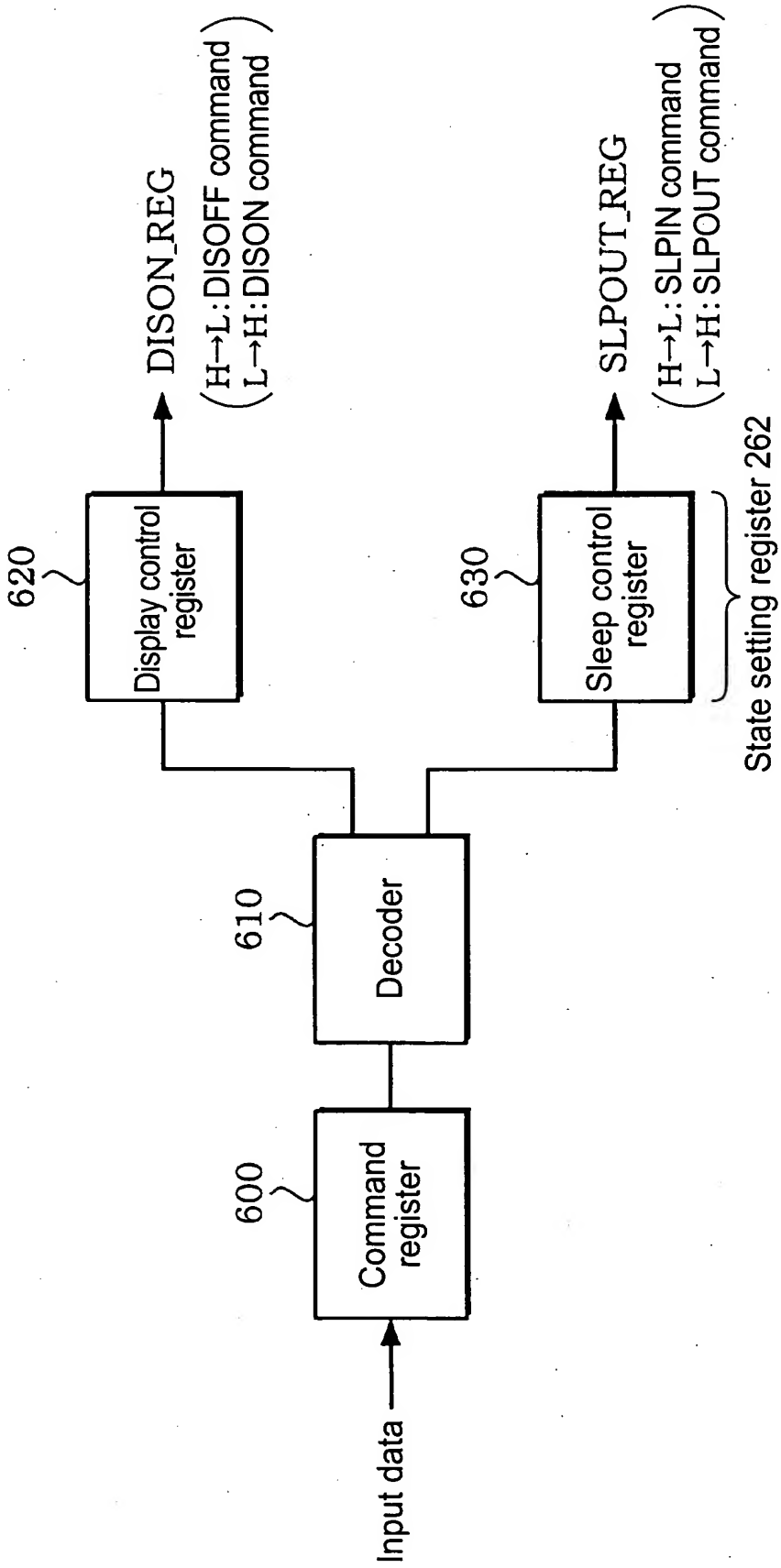
Input data
600
Command register
610
Decoder
620
Display control register
DISON_REG
(H→L:DISOFF command
L→H:DISON command)
630
Sleep control register
SLPOUT_REG
(H→L:SLPIN command
L→H:SLPOUT command)
State setting register 262

FIG. 7

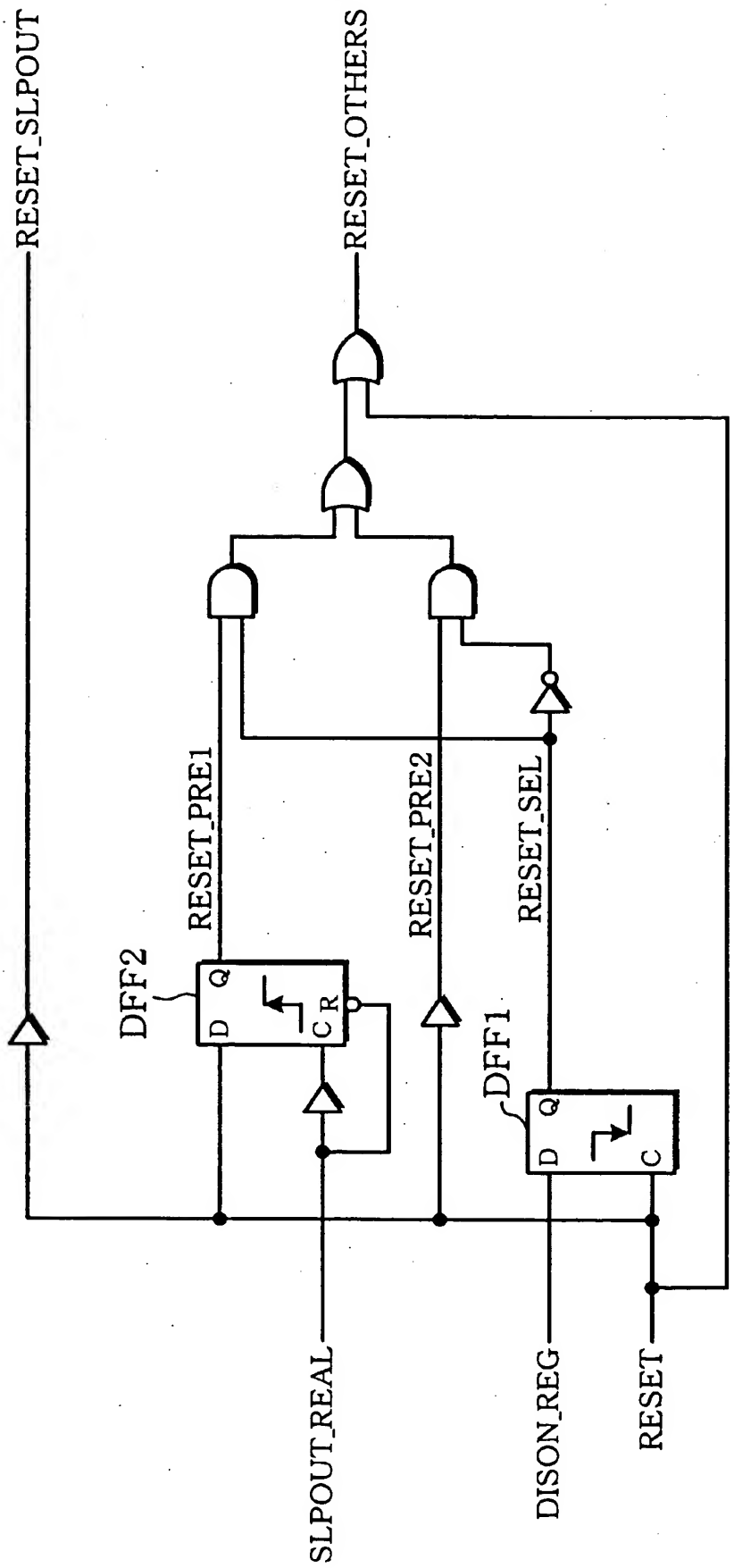
RESET_SLPOUT
RESET_OTHERS
RESET_PRE1
RESET_PRE2
RESET_SEL
DFF2
DFF1
D
Q
C
R
SLPOUT_REAL
DISON_REG
RESET

FIG. 8

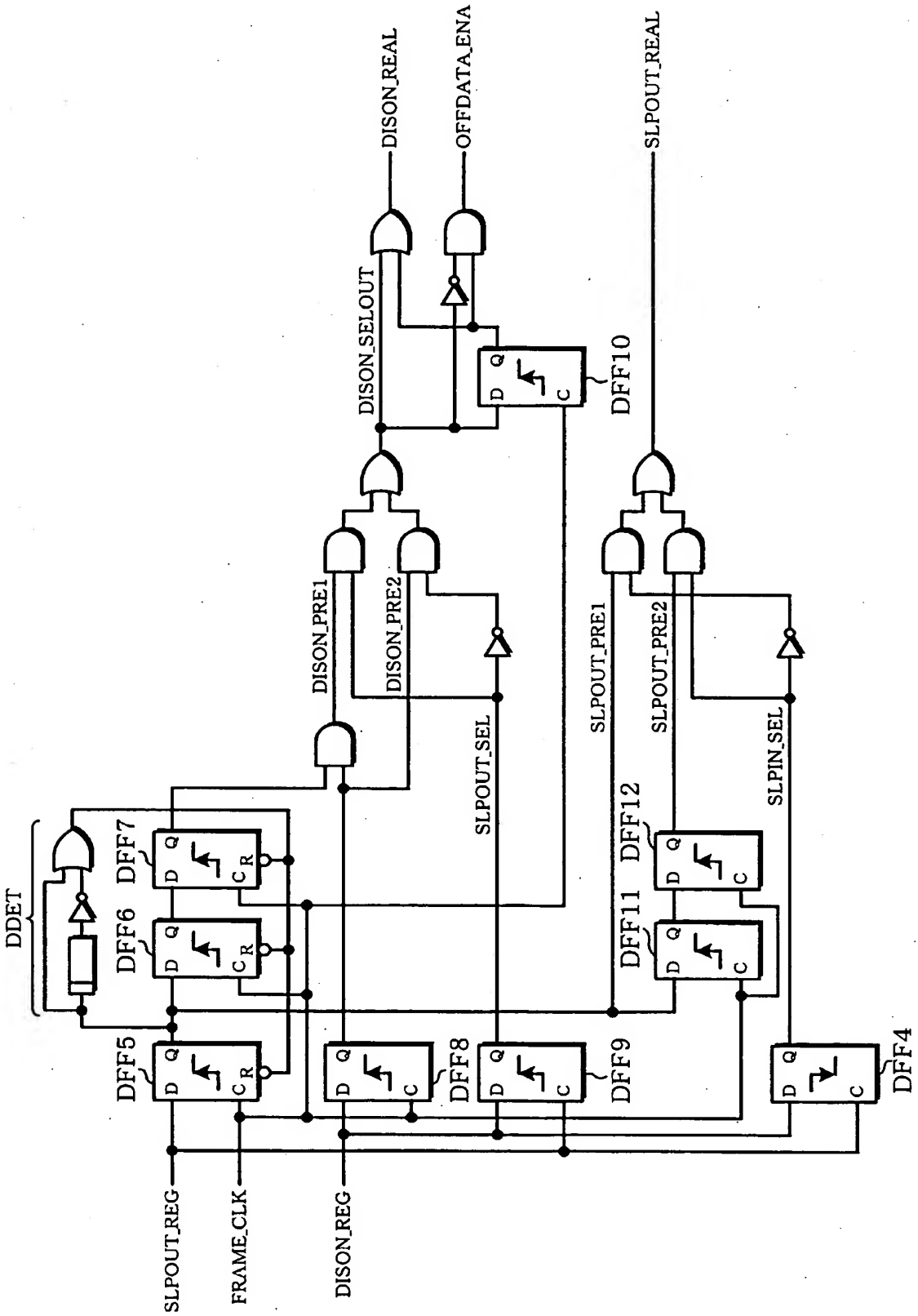
DISON_REAL
OFFDATA_ENA
SLPOUT_REAL
DISON_SELOUT
DFF10
DISON_PRE1
DISON_PRE2
SLPOUT_SEL
SLPOUT_PRE1
SLPOUT_PRE2
SLPIN_SEL
DDET
DFF7
DFF6
DFF5
DFF8
DFF9
DFF12
DFF11
DFF4
SLPOUT_REG
FRAME_CLK
DISON_REG

FIG. 9

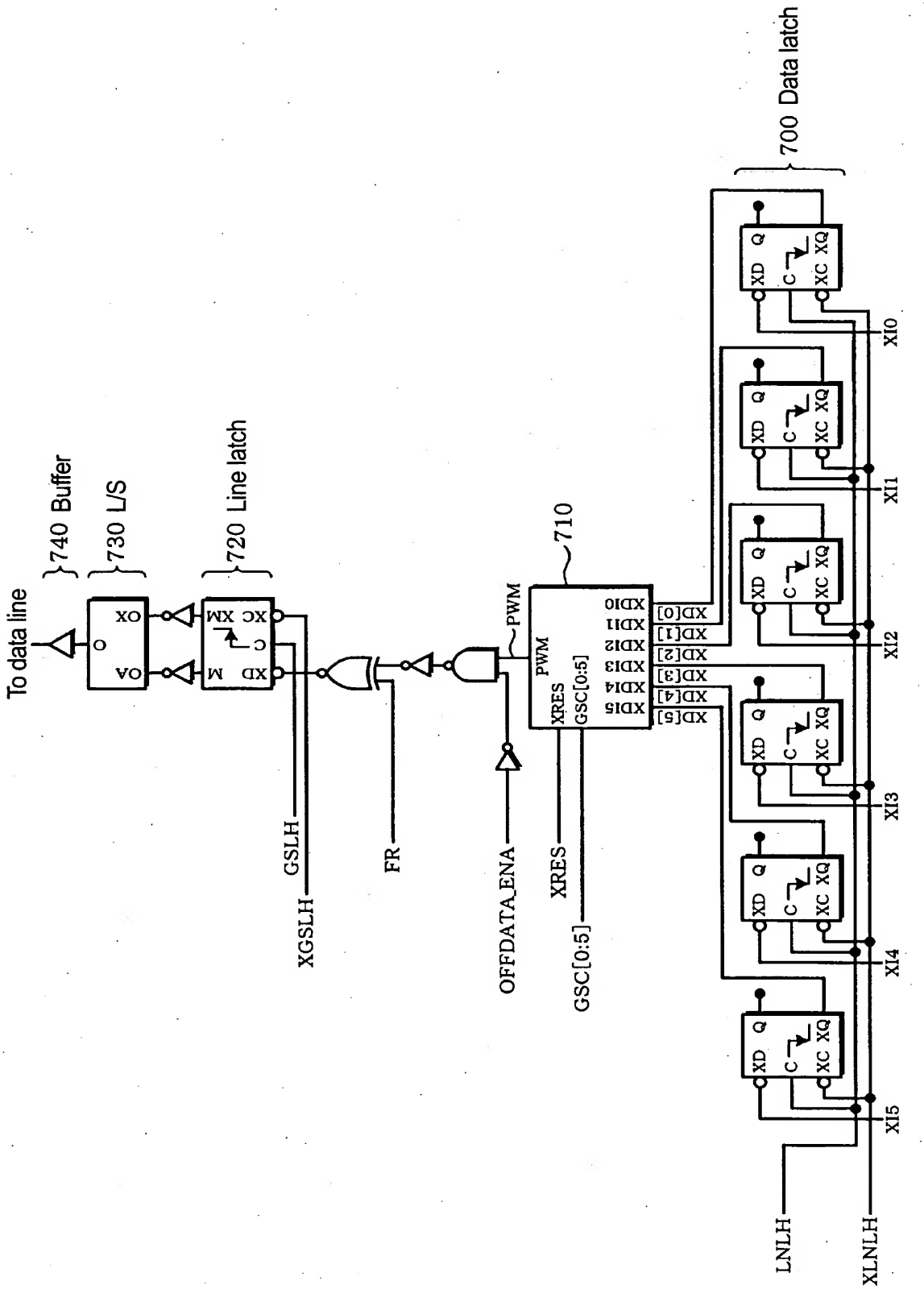
To data line
740 Buffer
730 L/S
720 Line latch
710
700 Data latch
PWM
XRES
GSC[0:5]
GSLH
XGSLH
FR
OFFDATA_ENA
XRES
GSC[0:5]
LNLH
XLNLH
XI0
XI1
XI2
XI3
XI4
XI5

FIG.10

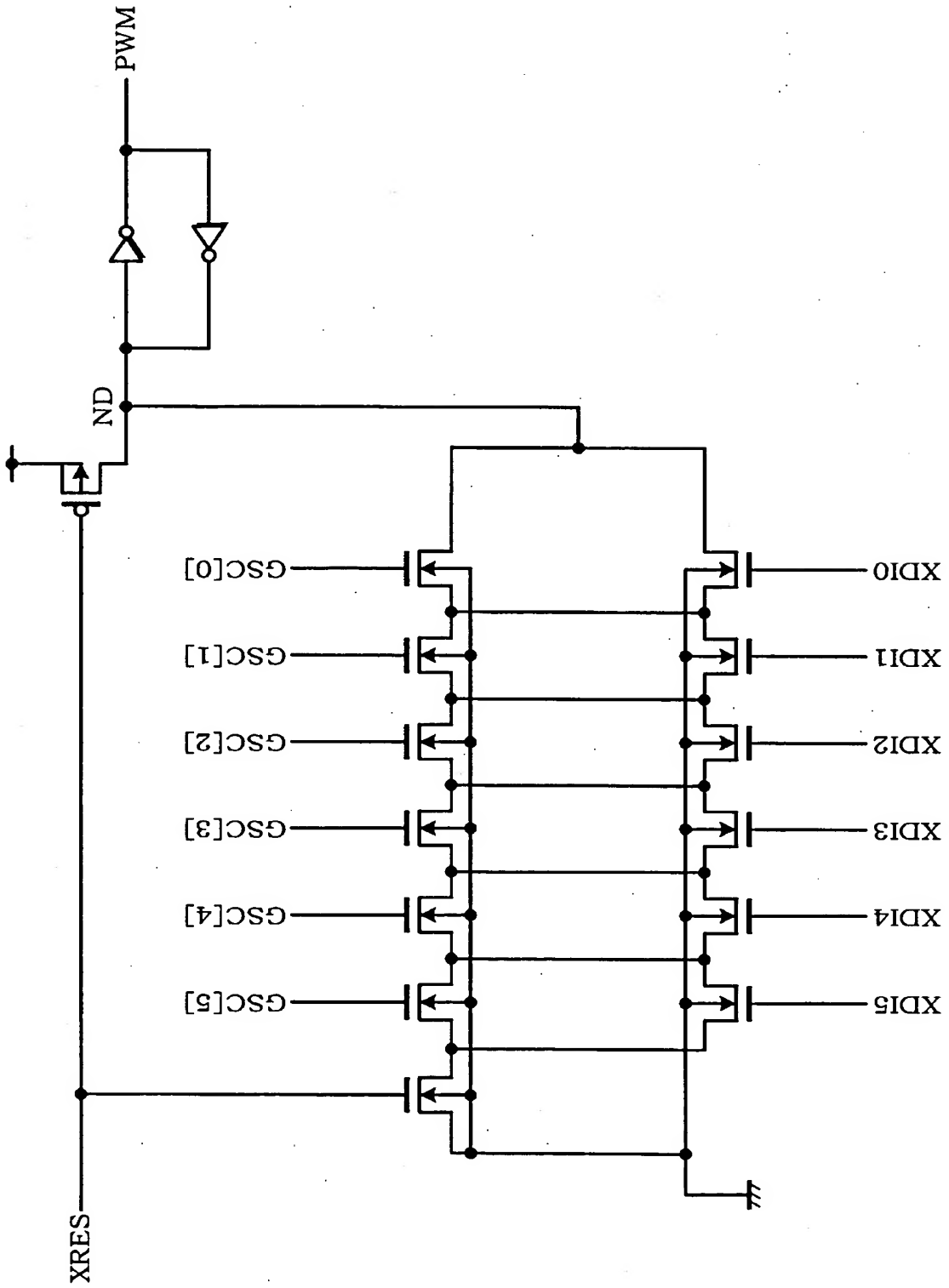
PWM
ND
GSC[0]
GSC[1]
GSC[2]
GSC[3]
GSC[4]
GSC[5]
XDI0
XDI1
XDI2
XDI3
XDI4
XDI5
XRES

FIG.11

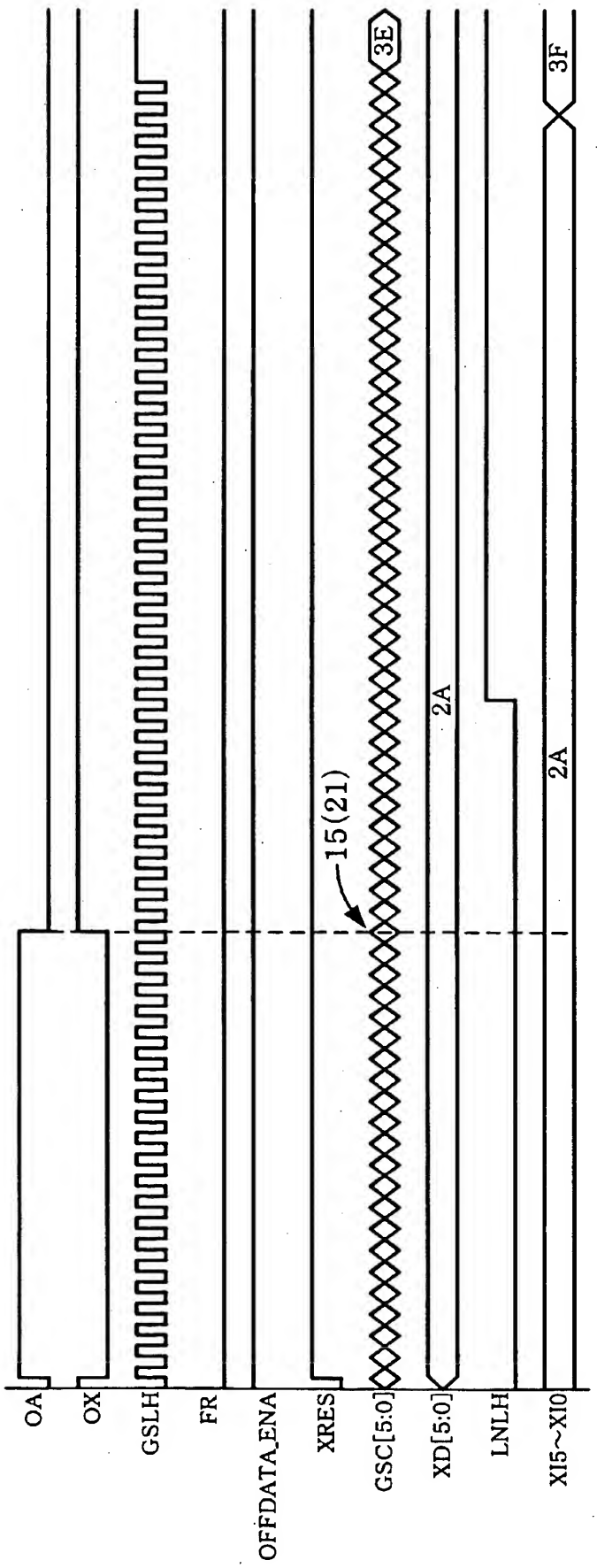
OA
OX
GSLH
FR
OFFDATA_ENA
XRES
GSC[5:0]
XD[5:0]
LNLH
XI5~XI0
15(21)
3E
2A
2A
3F

FIG.12

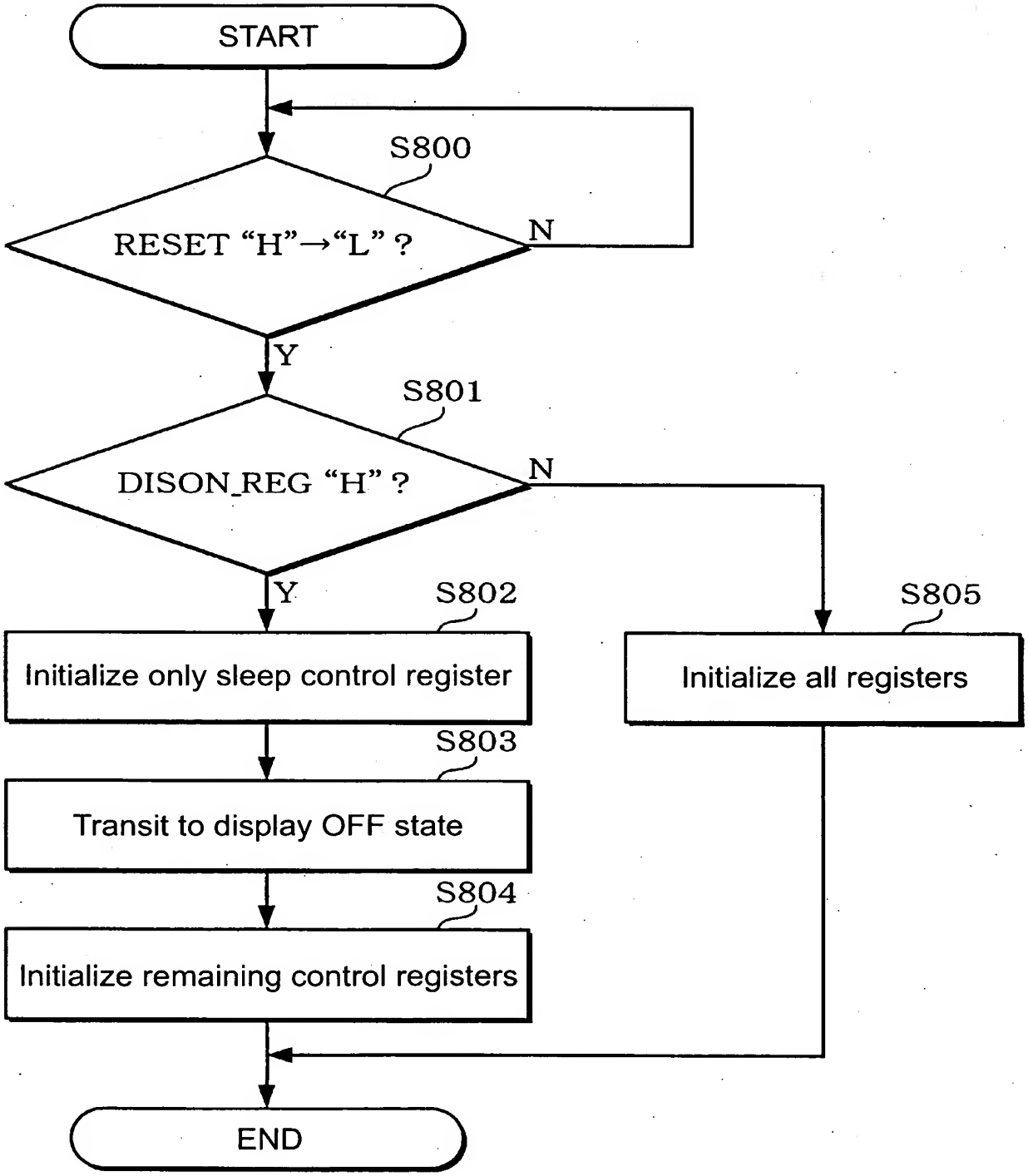
START
S800
RESET "H"→"L" ?
N
Y
S801
DISON_REG "H" ?
N
Y
S802
Initialize only sleep control register
S803
Transit to display OFF state
S804
Initialize remaining control registers
S805
Initialize all registers
END

FIG.13

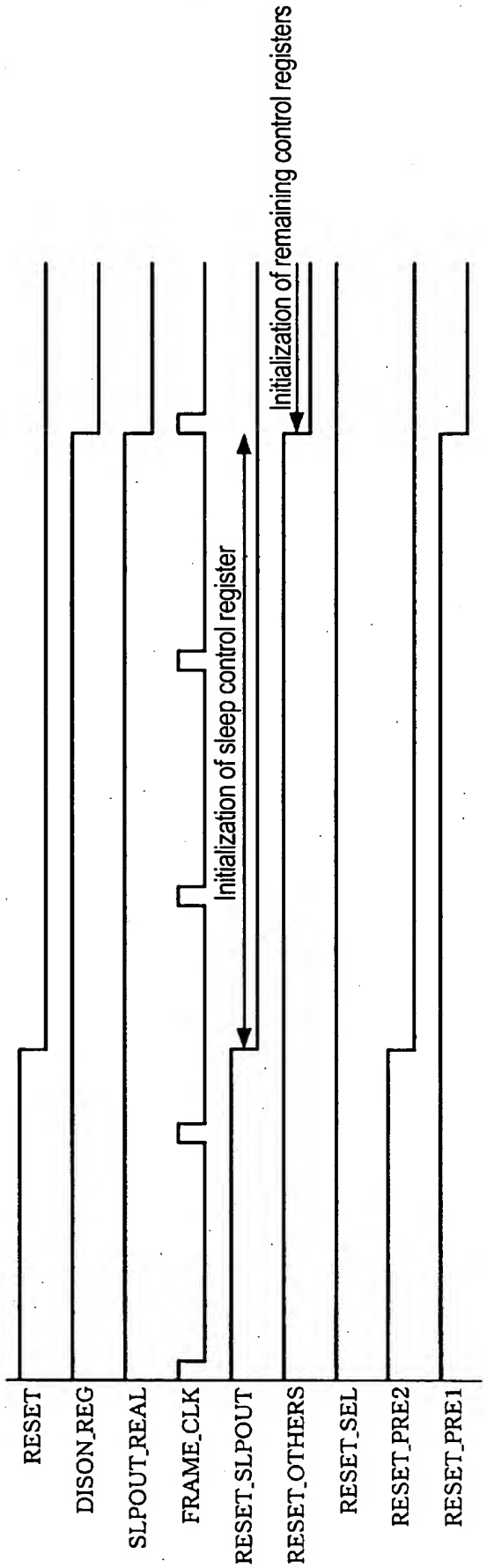
Initialization of remaining control registers
Initialization of sleep control register
RESET
DISON_REG
SLPOUT_REAL
FRAME_CLK
RESET_SLPOUT
RESET_OTHERS
RESET_SEL
RESET_PRE2
RESET_PRE1

FIG.14

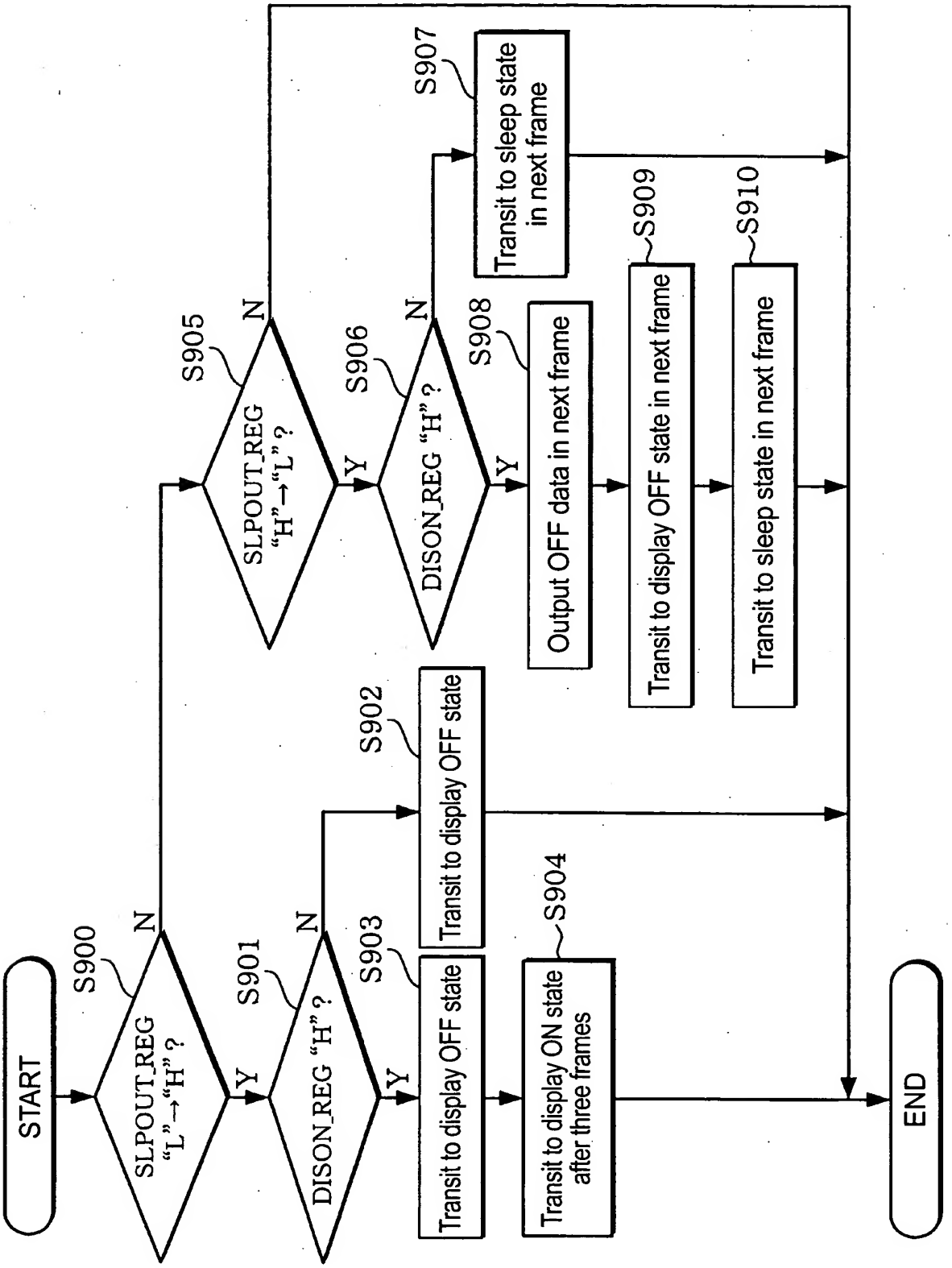
START
S900
SLPOUT_REG "L"→"H"?
N
Y
S901
DISON_REG "H"?
N
Y
S902
Transit to display OFF state
S903
Transit to display OFF state
S904
Transit to display ON state after three frames
S905
SLPOUT_REG "H"→"L"?
N
Y
S906
DISON_REG "H"?
N
Y
S907
Transit to sleep state in next frame
S908
Output OFF data in next frame
S909
Transit to display OFF state in next frame
S910
Transit to sleep state in next frame
END

FIG.15

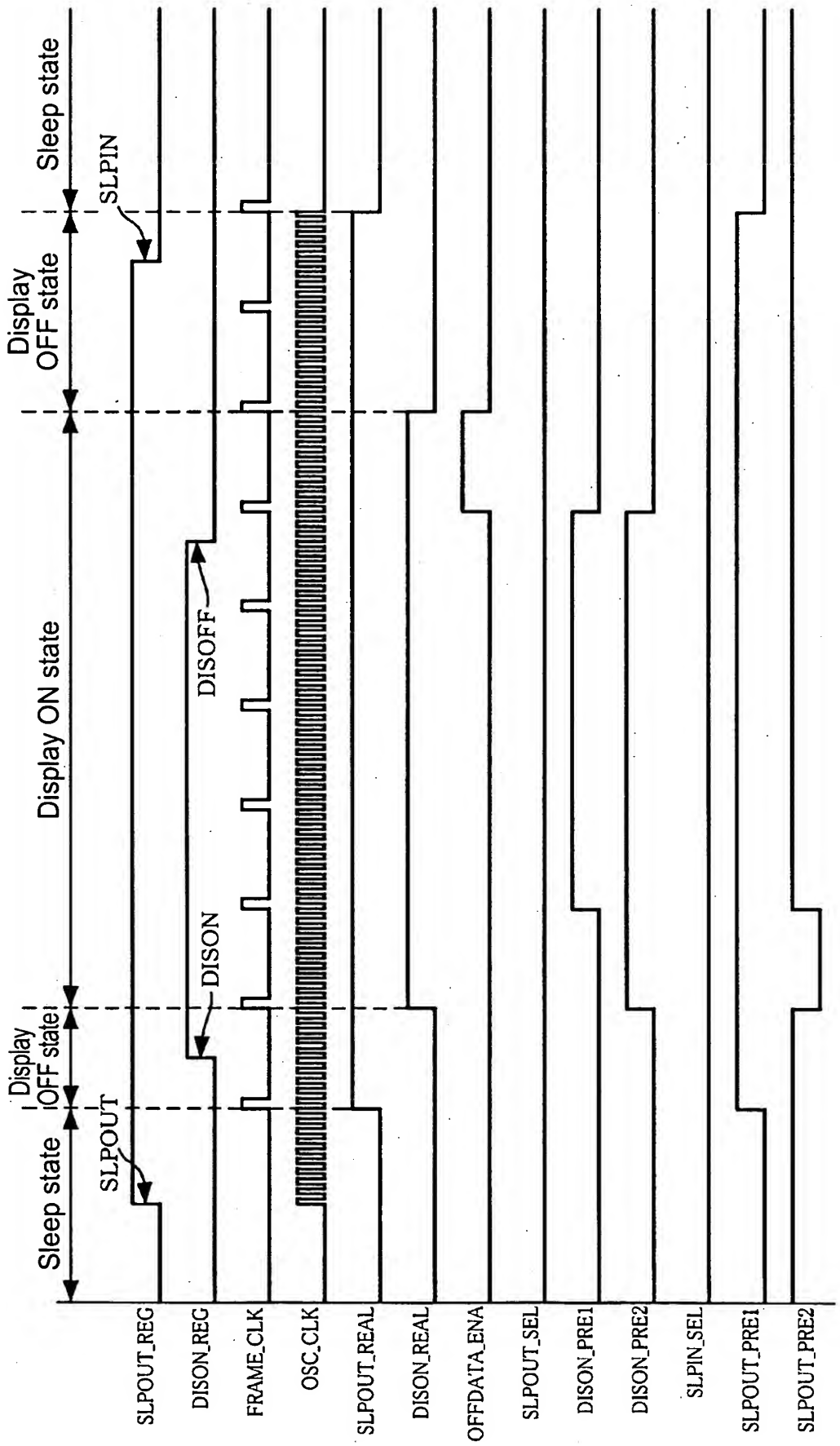
Sleep state
SLPIN
Display OFF state
Display ON state
DISOFF
DISON
Display OFF state
SLPOUT
Sleep state
SLPOUT_REG
DISON_REG
FRAME_CLK
OSC_CLK
SLPOUT_REAL
DISON_REAL
OFFDATA_ENA
SLPOUT_SEL
DISON_PRE1
DISON_PRE2
SLPIN_SEL
SLPOUT_PRE1
SLPOUT_PRE2

FIG.16

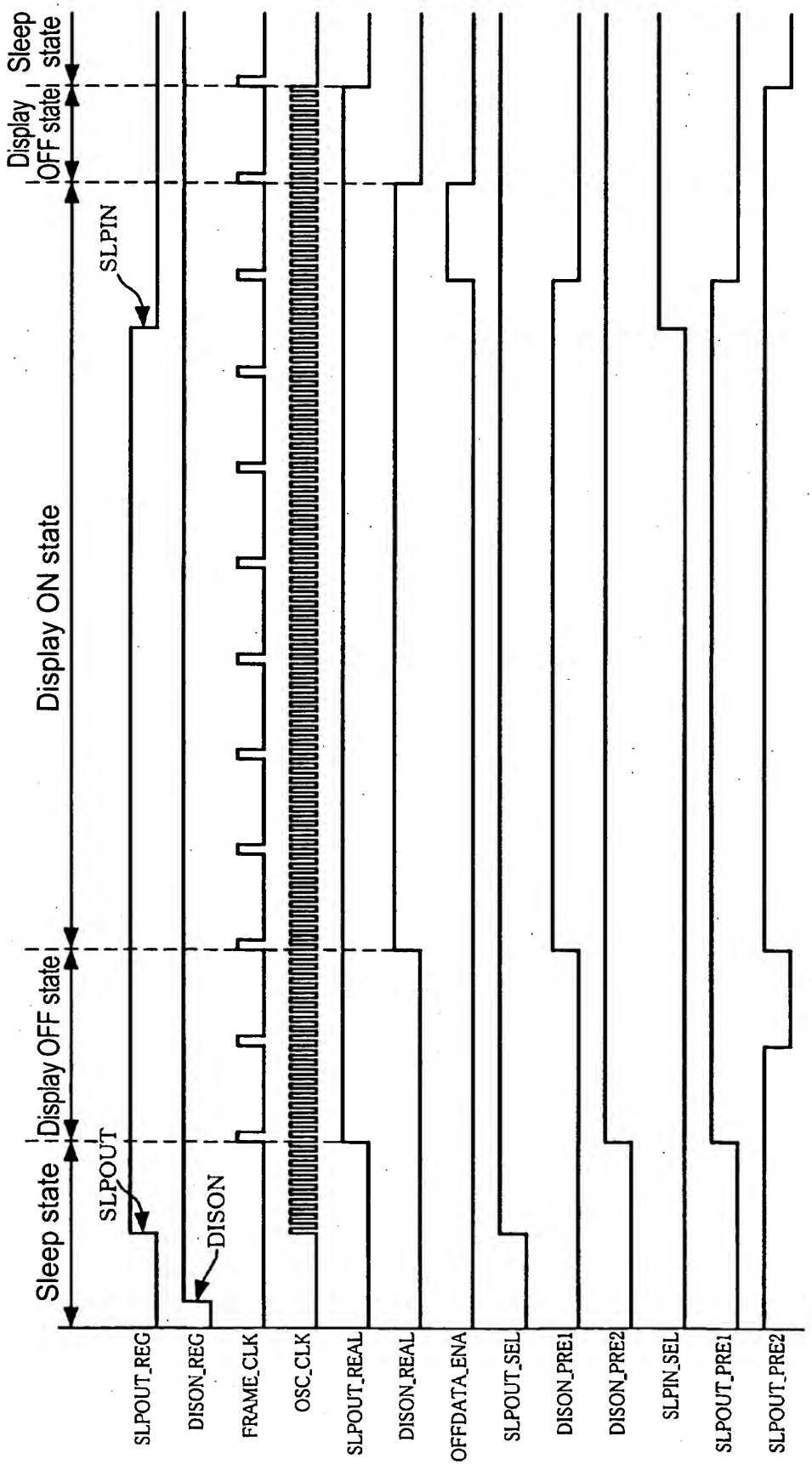
Sleep state
Display OFF state
Display ON state
Display OFF state
Sleep state
SLPIN
SLPOUT
DISON
SLPOUT_REG
DISON_REG
FRAME_CLK
OSC_CLK
SLPOUT_REAL
DISON_REAL
OFFDATA_ENA
SLPOUT_SEL
DISON_PRE1
DISON_PRE2
SLPIN_SEL
SLPOUT_PRE1
SLPOUT_PRE2

FIG.17